

CMOS Imager Design for Fast Centroid Readout

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Abstract

Numerous applications of imaging systems involve the determination of the centroid location of a localized region of high intensity (a "spot") that is easily distinguished from the background. The goal of the present work was to tailor the design of a custom CMOS imager to facilitate the centroid-location task. On-pixel circuitry, readout methods, on-chip post-readout processing and other factors were considered in the design process. The 'design process' included system modeling, simulation and experimental validation as well as chip-level design.

A triangulation rangefinder instrument was constructed to evaluate imager alternatives. The precision of the range determination is proportional to the precision of the location of the centroid of the image of an optical spot.

Range measurements are presented to demonstrate that uncertainty in centroid position, the dominant error source, can be significantly reduced by averaging. A novel CMOS imager design concept is described. Using on-chip processing and a 'pixel-binary', row/column-parallel readout scheme, range values are expected to have an update rate as high as 1 MHz. Key aspects of the chip design are evaluated, especially as they pertain to update rate and the use of on-chip averaging to enhance precision.

Keywords: CMOS, imager, binary, centroid, rangefinder.

1. INTRODUCTION

The determination of the centroid of a well-delineated, localized object (a 'spot') is an important aspect of many imaging applications. Figure 1(a) shows one such application, in which a small 'range object' is illuminated by an optical pulse [1]. Diffusely-reflected light from the

range object is collected by suitable optics and detected by an imaging array. The position of the image spot allows the range to be determined by triangulation, based on a known separation between the light source and the detector array. In Figure 1(b), the rangefinder subsystems are shown, grouping together the functions that can be readily integrated onto a common CMOS chip.

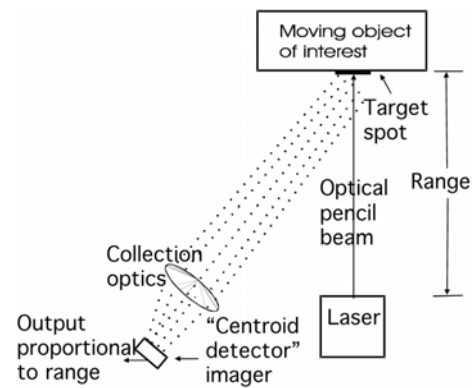


Figure 1(a) Representative Application: Triangulation Rangefinder

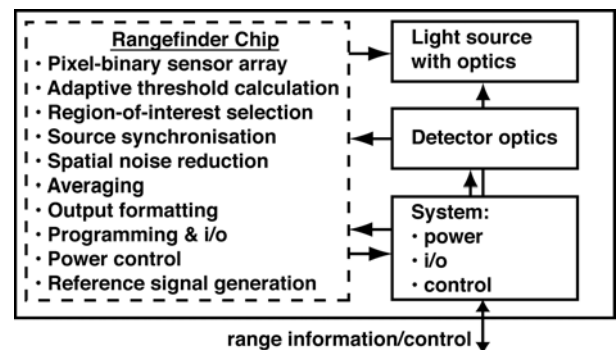


Figure 1(b) Potential On-Chip Functions of Rangefinder

A prototype rangefinder was implemented using a conventional CMOS imager, and evaluated for precision and accuracy. Only motions along the ‘range direction’ were considered. The averaging of $10^1 - 10^4$ or more successive image frames was shown to reduce by approximately \sqrt{n} the uncertainty in the centroid determination, which is the principal source of measurement error. For pixel centroid uncertainty below 0.01 pixel, systematic errors such as temperature drift, sub-pixel nonlinearity and array nonuniformity may become important [2]. A high frame rate is thus important for the attainment of enhanced precision while still following the location of a moving object. The use of synchronized laser illumination allows adequate optical signals for even sub-microsecond frame exposure periods in some scenarios, despite the relatively low sensitivity of CMOS imagers.

With a conventional CMOS imager, a range sensitivity of better than $\pm 1 \mu\text{m}$ at a range of 200 mm was achieved. This level of precision required the averaging of 10^2 images, showing that the refresh rate for range information must be traded off against precision. For conventional CMOS imagers, the frame rate is limited to about 10^2 to 10^3 Hz.

2. CMOS Pixel-Binary Chip Operation

A novel ‘pixel-binary’ CMOS imager has been developed. As illustrated in **Figure 2**, each pixel of the ‘pixel-binary’ imager has a comparator to provide a digital output for the pixel. Feeding the comparator are a conventional photodiode, a source-follower and additional circuitry for pattern-noise correction [2], [3]. For conventional readout and testing, the analog level is also available.

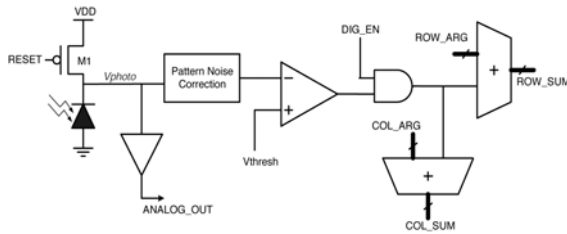


Figure 2 Representative Pixel Schematic for Pixel-Binary Imager

Various readout schemes are possible. For the pixel circuit of **Figure 2**, the digital signals in the rows and columns can be connected in a ‘wired-OR’ configuration or summed by in-pixel adders. With a well-defined, isolated spot image, this ‘cumulative cross section’

(CCS) output on the rows and columns can be read out in series or combined using on-chip logic (**Figure 3**) to give a centroid location.

The pixel-binary readout has been measured to give a centroid location with a precision of about ± 0.3 pixel for a single frame, limited by the threshold voltage and the number of pixels in the spot. Averaging and threshold variation can reduce the uncertainty by a factor of 10 to 100 before systematic errors become important. Temperature drift, detector defects, detector nonlinearities and mechanical deformations are the principal sources of systematic errors.

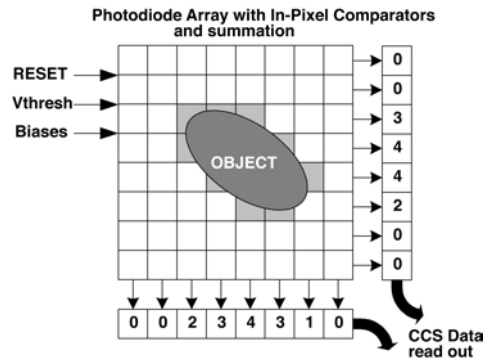


Figure 3 Pixel-Binary Readout Options for Centroid Location

The rate at which the centroid value changes at the output of the chip is governed by settling times within the pixel and by propagation delays/bus capacitance in the on-chip digital circuitry. Although limited to about 0.1 MHz in the current, proof-of-concept prototype device, the frame rate is expected to be significantly higher – in excess of 1 MHz – when the chip is optimized for speed.

For the current experiments, the outputs of the rows and columns are sent to an external computer. This computer interprets the data to determine the centroid location and the range, averages sequential values of range and synchronizes the light source and detector array.

The threshold voltage level for the pixel comparators is common to all pixels. Enhanced precision in the determination of centroid location is achieved by the acquisition of a series of images with different threshold voltages and also by the averaging of location values.

Table 1 shows the results of modeling and selected tests performed on the current version of the pixel-binary imager chip. In this version, two 6-bit adders were placed on each pixel and the row- and column-sum registers were read out in series. An off-chip computer calculated the centroid position for each frame and performed the averaging of location values. (The on-chip

implementation of such functions was deemed to be straightforward.)

Comparator bias current was calculated to dominate power dissipation for operating speeds below 10 MHz. Preliminary tests indicated a DC quiescent current of about 10^{-4} to 10^{-3} A. This leakage current is attributed to design and manufacturing artifacts; power minimization was not a design driver in the current chip.

Table 1 Characteristics Measured on Current Prototype Pixel-Binary Imager

Param	Units	Meas value	Model value	Notes
Power	W /pixel	10^{-5}	10^{-6}	for 'enabled' pixels
# of pixels	-	4096	10^4	1.6 mm pixel region on die
Pixel size	μm	-	25.5	By design
settling time	μs	<10	1 - 10	comparator [2], adder chain
centroid rate	MHz	-	0.1	Iterative on-chip centroid location
V_{thresh} change	μs	-	3	Potential limiting factor
Sensitivity	V/lux /sec	0.2	1	Standard 0.18 μm CMOS [5]
Dynamic range	dB	12	10	pixel tradeoffs [5]
Sub-pixel linearity	%	4	-	Due to fill factor [2]
Fill factor	%	-	27	0.18 μm features, on-pixel adders

The "centroid rate" in **Table 1** is limited by the on-chip analog and digital settling times, the readout, the on-chip erosion algorithm for centroid location and the speed of the external computer or other electronics used for averaging. Many of these factors are not intrinsic to the present fast-chip concept, and the frame rate can be significantly increased by modifications to the chip design.

The settling time of the readout path will be measured with a $1 \mu\text{A}$ bias current, which is considered to be a reasonable tradeoff between power dissipation and speed for this device. Larger bias currents can reduce the settling time, may be appropriate for higher-speed operation and may require reduced fill factor or other pixel/comparator optimizations.

The useful dynamic range of the input signal, defined here as the ratio of the saturation level to the RMS noise, depends on the random noise, spatial inhomogeneities and photoresponse sensitivity. In the pixel-binary mode of operation, the dynamic range was considered as a constraint on the tuning range of the comparator

threshold voltage, V_{thresh} , and was treated as a secondary design parameter compared to settling time and circuit layout factors. (The "circuit layout factors" include line width, capacitance, leakage, mask errors, layout area, digital and analog crosstalk and considerations of the effect of lateral diffusion and fill factor on the modulation transfer function.) Fill factor affects sensitivity and may cause sub-pixel nonlinearity. The number of adder bits affects fill factor and may influence the on-chip processing.

3. Fast-Readout Pixel-Binary Imager Design

A conceptual design has been created for a CMOS imager that implements centroid location at an enhanced rate and incorporates on-chip 'cumulative cross section' (CCS) centroid calculation and averaging (**Figure 4**).

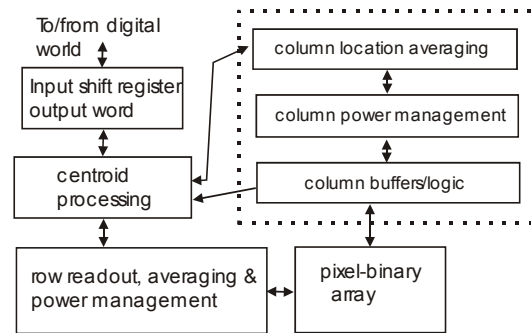


Figure 4 Block Schematic of Main Elements of a Centroiding Imager

Based on the aforementioned measurements and modeling with a conventional imager in a rangefinder, it is deemed useful to incorporate averaging onto the chip. An average can be implemented by summing the location values, then reading out the appropriate bits of the sum-word. Alternatively, the summations can be performed on the row-sum and column-sum registers before the location-determination logic. Additional logic can allow offset compensation, velocity readout, synchronous detection and linear transformation for direct range readout.

Power management can be implemented by turning off the comparators that are not in the selected region of interest. This method also reduces the length of the row- or column-sum register that needs to be read out or processed for centroid location. For flexibility, an input control buffer is useful. The output can be a single signal line with serial access to the row- and column-centroid words, or can include a parallel readout. By control-buffer reconfiguration, the amount of on-chip averaging or other operational parameters can be altered.

Preliminary modeling of a chip with megahertz-rate centroid output is in process. **Table 2** summarizes selected features planned for this chip.

Bus capacitance may be reduced by splitting the bus into multiple smaller buses. Logic to combine the buses in a hierarchical manner can be fast, low-power and of small area. The design concept allows other such tradeoffs between analog and digital implementation and in the location of digital circuits (on-pixel, associated with rows/columns or in post-readout processing). Power versus speed in the pixels is a tradeoff that can be optimized by power-control strategies, ROI operation, pixel design and layout.

Table 2 Selected Features of New Chip Design

feature	Description/rationale
Row/column power control	Region of interest; noise suppression; low power
Revised algorithm for centroid	10x increase in output rate
Buffered comparator reference voltage	Faster variation of threshold
On-chip location sums	Averaging at full information rate; velocity readout
Isolated-event logic	Noise suppression
Chip-average photo-signal	Assists in setting of comparator voltage
Adaptive comparator voltage	To set the threshold in the preferred region for spot/not-spot discrimination
Adaptive ROI power control	To reduce power and noise
Enhanced on-pixel circuitry	To speed pixel analog and digital response
Enhanced row/column readout buses	Reduced capacitance, for shorter settling times, for analog. For digital, use a summing tree.
Linear transformation	Converts centroid-location output to range
On-chip time stamp	To facilitate velocity meas., and multi-camera synthesis

The arrival time of an “event” can be accurately timed using a pixel-binary imager. This capability plus on-chip arithmetic logic, allow accurate velocity calculations. A timing output can also facilitate the synchronization and synthesis of imagery from a network of cameras.

To push the centroid update rate to much beyond 10 Mhz is expected to be constrained by additional parameters such as transistor settling times, bus and component propagation delays, chip-dimension effects and the time needed for on-chip post-processing. For

instance, the digital delays in the current adder (on each pixel) is about about 2×10^{-9} s. While negligible for even 1 MHz operation with 100 pixels per readout ‘line’, this delay may be significant for higher frame rates or larger ROI.

Implementation of this chip is planned in the TMSMC 0.18 μm CMOS process provided by the Canadian Microelectronics Corporation (CMC). Due to the size constraints imposed by the implementation strategy, not all of the desired features can be implemented on-chip at the present technology level. Some features can, initially, be placed on an FPGA or similar device to achieve the update rate objective. As feature sizes shrink, the overall performance of the fast-centroiding chip is expected to improve and on-chip logic takes up even less power and chip area. Active illumination and improved fill factor should compensate for degradations in photo-response.

4. CONCLUSIONS

Guided by measurements and modeling with conventional cameras and the characterization of a custom CMOS imager chip, the design concept for a megahertz-rate, high-precision centroid-readout imager has been developed.

Acknowledgements

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