A Double-Delta Compensating Technique for Pulse-Frequency Modulation CMOS Image Sensor

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Abstract—We design a double-delta compensating (DDC) technique for a comparator-based pulse-frequency modulation (PFM) pixel. This technique has been demonstrated by simulation to achieve both fixed-pattern noise (FPN) reduction and dynamic range (DR) extension at the high-light region. According to the result, the pixel DR extends by at least 12 dB; FPN is reduced from unacceptable levels to 1–3% when it is caused by the comparator offset voltage or less than 3.5% when the layout and process variations are considered. These simulations have been performed using the Monte Carlo method for realistic parameter variations in a 0.18-µm CMOS technology.

I. INTRODUCTION

Recently, pulse-frequency modulation (PFM) or pulse-width modulation (PWM) pixels have been developed with a target of wide dynamic range (WDR) imaging applications [1]–[4]. Their typical structure uses a sigma-delta (Σ-Δ) operand, normally a single-ended comparator, to perform a light-to-frequency conversion. Due to the multiple self-reset operation, dynamic range (DR) is not limited by the full-well capacity of the photodiode and the available DR is over 100 dB with standard CMOS technologies. However, the PFM pixel is not greatly favored in practice due to its relatively poor pixel-wise fixed-pattern noise (FPN), which is reported to be more than 5% [2], [4]. In the typical active pixel sensor (APS), this issue is solved by the correlated-double sampling (CDS) technique [5], but this approach is not directly applicable to the PFM pixel. In addition, the high-light imaging range is degraded by the duration of the reset period, which increases with the illumination [6]. This problem is directly associated with the propagation delay of comparator and is not easily solved with current CMOS technologies.

The block diagram of a regular PFM pixel is shown in Fig. 1. The output pulse frequency is determined by \( I_{ph}/(C_{PD} \cdot V_{diff}) \), where \( I_{ph} \) is the photocurrent, \( C_{PD} \) is the photodiode capacitance, and \( V_{diff} \) is the difference between the reset \( (V_{rst}) \) and reference \( (V_{ref}) \) voltages. Apparently, in order to generate a higher output frequency which is preferred by many applications, a smaller \( V_{diff} \) is necessary. However, the two issues mentioned above will be seriously affected by the smaller \( V_{diff} \) [6]. First, the offset voltage of the comparator \( (V_{off}) \) has a normal distribution and is in the range of 5–15 mV depending on the circuit design, layout strategy, and process control. Although comparator designs with low offset voltage are available [7], [8], they are not directly usable by the PFM pixel due to their complexity or their operational mechanisms. Therefore, once \( V_{diff} \) gets smaller, the mismatch-induced offset becomes relatively large and greatly increases the FPN. Second, the smaller \( V_{diff} \) results in a smaller integration-to-reset ratio within one pulse period, which turns off the operation of PFM pixel when the reset period becomes greater than the integration period [6]. The high-light DR is therefore sacrificed. As a result, an approach that solves the problems of using a small \( V_{diff} \) is necessary to better utilize the PFM pixels.

In this paper, we propose a double-delta compensating (DDC) technique in an effort to reduce the FPN and extend DR for the comparator-based PFM pixels. The DDC technique is simulated to verify its feasibility in a 0.18-µm CMOS process. From the simulation results, the technique noticeably extends DR by at least 12 dB and reduces the FPN to an acceptable level. The following context will introduce the idea of the DDC technique and its circuit realization. Several simulation scenarios are included to support the idea and provide useful information for future chip implementation.

II. DOUBLE-Delta COMPENSATING TECHNIQUE

The concept of the DDC technique is described as follows. For a regular PFM pixel, the reset operation is usually repeated many times in one single frame. Therefore, any existing \( V_{diff} \) in the comparator will change the original \( V_{diff} \) to \( (V_{diff} \pm V_{off}) \), and the resulting pixel output frequencies will vary over the entire pixel array. Since \( V_{diff} \) of the comparator is often regarded as a voltage source at one of the two input nodes, it can actually be compensated within every two consecutive integrations if the connections between the signals \( (V_{PD} \) and \( V_{ref} \)) and the inputs as well as the polarities of comparator are both switched. This idea is illustrated in Fig. 2 and its functionality will be explained below.
**A. FPN Reduction**

In Fig. 2, when the integration begins, the pixel is at the initial state (Mode 1). Since an offset voltage is attached to the positive input of comparator to approximate the real condition, the actual integration voltage is \( V_{\text{diff}} \) plus \( V_{\text{off}} \). Thus, the potential of \( C_{\text{PD}} \) has to change an amount of \((V_{\text{diff}}+V_{\text{off}})\), or \( V^+ \), to trigger the comparator. Once the integration completes and the trigger signal is sent, the input connections and the polarities of comparator are both exchanged, and the pixel is in another state (Mode 2). Therefore, the next integration will have an integration voltage of \( V_{\text{diff}} \) minus \( V_{\text{off}} \), and the potential drop of \( C_{\text{PD}} \) has to be \((V_{\text{diff}}-V_{\text{off}})\), or \( V^- \), to trigger the comparator. After the second integration finishes and another trigger signal is generated, the input connections and the polarities of comparator will be switched again (Mode 1). As the procedure repeats, every two integrations will have a total integration voltage given by

\[
V^+ + V^- = (V_{\text{diff}} + V_{\text{off}}) + (V_{\text{diff}} - V_{\text{off}}) = 2 \cdot V_{\text{diff}}.
\]

(1)

According to (1), \( V_{\text{off}} \) is cancelled within two integrations using the DDC technique. In Fig. 3, the \( V_{\text{off}} \) compensation is further illustrated where an ideal integration voltage \( (V_{\text{ideal}}) \) and two practical with \( V_{\text{off}} \) (\( V_{\text{PD1}}, V_{\text{PD2}} \)) are plotted. When the DDC technique is not used, the output frequencies change with the varying \( V_{\text{off}} \) (the dotted lines of \( V_{\text{PD1}} \) and \( V_{\text{PD2}} \)). By applying this technique, \( V_{\text{off}} \) is compensated within every two consecutive integrations, and the average frequencies of \( V_{\text{PD1}} \) and \( V_{\text{PD2}} \) will equal that of \( V_{\text{ideal}} \) regardless of the value of \( V_{\text{off}} \) (the solid lines). As a result, FPN is suppressed when the DDC technique is utilized in the PFM pixels.

**B. DR Extension**

DR extension achieved by the DDC technique can be explained by the illustrations in Fig. 4. In these figures, the voltages at the integration node (\( V_{\text{PD}} \)), the comparator output (\( V_{\text{comp}} \)), and the gate of reset transistor (\( V_r \)) are magnified to show the details of reset operation. In Fig. 4(a), when the reset starts \((t_1)\), \( V_{\text{PD}} \) is charged by the reset current. The reset is completed in a very short period where \( V_{\text{PD}} \) is pulled up across \( V_{\text{ref}} \) and reaches \( V_{\text{comp}} \), and forces the comparator to output a low \((t_2)\). However, \( V_r \) will not be turned off until another period of time \((t_3-t_2)\) has passed where \( V_{\text{comp}} \) is below a threshold \([1/2]V_{\text{DD}}\). In [6], this period is found to be dominated by the propagation delay of the comparator, and it becomes longer when the intensity of illumination increases. As a result, the pulse period will be seriously affected by the reset period in high-light conditions, and DR is constrained.

By implementing the DDC technique, the usually overlong reset period can be reduced. In Fig. 4(b), the reset operation is identical to that of Fig. 4(a) when the reset starts \((t_1')\) and \( V_{\text{PD}} \) is reset to \( V_{\text{off}} \) \((t_2')\). After the reset is done, the added DDC technique will exchange the polarities of comparator, so its reset period will be shortened by skipping the propagation delay of comparator. Note the best time for the switching to occur is the moment the reset is complete. The switching will make \( V_{\text{comp}} \) drop quickly to \((1/2) V_{\text{DD}} \) without being delayed, and \( V_r \) is turned off right after the reset completes. Therefore, the reset period is reduced from \( t_3-t_1 \) to \( t_3'-t_1' \). Accordingly,
the reset period will be less prominent when the illumination gets strong (the integration period is short), and DR can be extended into this high-light region.

### III. Circuit Implementation

The block diagram of the proposed PFM pixel is shown in Fig. 5. The implementation of switchable input nodes requires four transistors to change between the two modes shown in Fig. 2. A switched-polarity comparator is also designed to accomplish the DDC technique. Based on one of the conventional comparator structures used in the PFM pixels [Fig. 6(a)] [4], a modified structure is proposed [Fig. 6(b)]. This design uses another four transistors to exchange the connections between the first and second stages of comparator, which changes its polarities while leaving V\textsubscript{off} where it is. This is designed on the assumption that the variation of the first stage is most critical to V\textsubscript{off}.

In the proposed designs of Fig. 5 and Fig. 6(b), one control signal (S), which changes its state every time a pulse signal is generated (i.e., one single reset occurs), is required. Since the PFM pixel signal can be recorded by the in-pixel counter [4], its least significant bit (LSB) precisely changes its state at the end of every integration and can be directly used for the control signal. As a result, no additional control signal is required, and the cost of implementing the DDC technique is only eight transistors (four for switching the input connections and four for switching signals inside the comparator).

### IV. Preliminary Simulation Results

The proposed PFM pixel with a switched-polarity comparator was simulated in a 0.18-\textmu{}m CMOS process, using the Monte Carlo method to simulate process variations. Each of the two parameter sets for the Monte Carlo simulations will be executed with 100 samples, and the variation of the average pulse width with respect to the ideal number (without V\textsubscript{off}) is calculated and treated as the FPN. In order to generate the highest output frequencies, V\textsubscript{off} is set at 0.01 V. This small value also best displays the impact of V\textsubscript{off} on the FPN. Furthermore, C\textsubscript{PD} is 100 fF, I\textsubscript{ph} is 5 fA–20 nA, and V\textsubscript{DD} (V\textsubscript{act}) is 1.2 V; the temperature is 40 degrees Celsius. The variations, which have a normal distribution, are summarized in Table I (3\sigma value is assigned a realistic value or calculated according to the library model).

#### A. FPN with V\textsubscript{off} Variations

Fig. 7 shows the simulation results using three different V\textsubscript{off} variations, including a 3\sigma value of 5 mV (□), 10 mV (∗), and 15 mV (△), respectively. The average FPNs for the baseline pixel (dotted lines) are between 5% and 15%, depending on the value of variations, which are unacceptably large. However, the FPN is reduced to 1–3% by using the proposed DDC technique (the solid lines), regardless of the value of variations. As a result, the V\textsubscript{off}-induced FPN is reduced to an acceptable level by compensating the variation within every two integrations. It is also notable that FPN without the DDC technique decreases until I\textsubscript{ph} is 100 pA and increases after that point. This is explained by the dominance changes of the integration and reset periods toward the total pulse width [6].

#### B. FPN with Width and V\textsubscript{th} Variations

Instead of using a simplified offset voltage source at the comparator input node, the layout and process variations are considered for all transistors in the pixel to more closely simulate the real condition. The selected parameters, width and V\textsubscript{th}, are usually the first to be considered for variation assessment. These variations are 2.52–12.6% for width and 2.8–19 mV for V\textsubscript{th}, depending on the size of each transistor. From the simulation results shown in Fig. 8, we find the DDC technique can reduce the FPN caused by the layout and process

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<th>Set</th>
<th>3\sigma</th>
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<td>V\textsubscript{off}</td>
<td>5, 10, and 15 mV</td>
<td>2.52–12.6%</td>
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Fig. 7. The FPN with different $V_{dd}$ variations. $3\sigma$ values are 5 mV (□), 10 mV (○), and 15 mV (+), respectively.

Fig. 8. The FPN with width and $V_{th}$ variations.

Fig. 9. The simulated transfer curves with and without the DDC technique, respectively. The result suggests a 12-dB DR extension.

Variations. The average FPNs are 3.5% and 10% for the PFM pixel with and without DDC technique, respectively.

C. Extended DR

In Fig. 9, the transfer curves of PFM pixel with and without implementing the DDC technique are plotted. From this figure, the conventional PFM pixel has an early saturation when $I_{ph}$ is about 1–5 nA due to the increasing reset period discussed in [6]. On the other hand, implementation of the DDC technique reduces the lengthy reset period, particularly at high illuminations, and the saturation happens beyond 20 nA. The DR extension is at least 12 dB, and the signal linearity is also improved. The highest output frequency is boosted to 20 MHz from the original 2 MHz.

V. Conclusion

A double-delta compensating technique for the PFM CMOS image sensor is proposed to reduce the FPN and increase DR. This method only requires eight additional transistors, where four of them are used for switching input connections, and the others in a switched-polarity comparator. Although eight extra transistors will significantly reduce the fill factor if the pixel pitch is small, this approach is still useful when the pixel is equipped with memory cell. This technique has been simulated using HSPICE and the Monte Carlo method in a 0.18-μm CMOS process. Various parameters, including the offset voltage as well as the transistor widths and threshold voltages, are used to verify the feasibility of this technique. According to the preliminary results, the DDC technique successfully reduces the FPN induced from the comparator offset voltage to 1–3%. That due to the layout and process variations is also reduced to an average of 3.5%. This technique also extends DR by at least 12 dB. In general, the DDC technique can be implemented with a minimum cost in any PFM pixel that uses a comparator.

REFERENCES