CMOS ACTIVE PIXEL IMAGE SENSOR WITH COMBINED LINEAR AND LOGARITHMIC MODE OPERATION

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ABSTRACT
An active photodiode 4 x 64 image sensor array was designed and fabricated using a 0.5 µm CMOS process. The sensor includes on-chip timing and control as well as correlated double sampling for readout. The operation of the sensor is selectable between a linear integration mode and a logarithmic mode using the same array of pixels.

INTRODUCTION
In recent years, CMOS image sensors have generated much interest for commercial applications. The major advantages of CMOS sensors are high level of integration, low voltage operation and low production cost, especially as the fabrication process moves towards deep sub-micron dimensions. Thus, it is possible to achieve much higher resolution on the same area with smaller pixels. Previous reports are mostly based on technologies of 0.8 µm or larger and it becomes important to investigate impact of new technology on sensor performance.

In this paper, a Hewlett-Packard 0.5 µm digital CMOS process (single poly, triple metal) is adopted for fabrication of the sensor. The design includes on-chip sample-and-hold circuits for readout and noise reduction and decoder circuits for array scanning. The pixel can be operated in either a linear integration mode or a logarithmic mode. Linear Integration mode operation of the sensor can achieve large output signals and thus a high signal-to-noise ratio. On the other hand, the logarithmic mode of pixel operation allows a wide dynamic range. Our design incorporates both modes of operation which can be selected by a control signal according to different applications.

SENSOR DESIGN AND OPERATION
The prototype sensor array consists of 4 rows of 64 pixels, with pixel size of a 30 x 30 µm. The sensor is operated by activating one row at a time with a row select transistor. Output signals from the pixels in the selected row are simultaneously transferred to sample-and-hold circuits from where they are readout by activating a column decoder. The automatic scan of the array is implemented by a counter which generates the address signals to the row and column decoders. The functional diagram of the sensor is shown in Fig. 1.

Simple photodiode is adopted as the photosensing element; schematic and layout views of the photodiode pixel are shown in Fig. 2 and Fig. 3, respectively. In each pixel, there are three transistors serving as pixel reset, source-follower amplifier and row select. The fill factor (defined as the fraction of the pixel area that is photosensitive) is about 60%. The non photo-sensing area is shielded by a metal 3 layer (not shown).
Correlated double sampling (CDS) is implemented using sample-and-hold circuitry, as shown in Fig. 4 [1]. The sampled signal is stored in capacitor $C_S$ by turning on transistor SHS. Then the pixel is reset and the resultant reset voltage is read out to capacitor $C_R$ by turning on transistor SHR. The output of the pixel is the difference between these two stored values. This reduces the fixed pattern noise arising from the mismatches between pixel components.

The timing diagram is shown in Fig. 5. The period of the pixel integration time is proportional to column readout signal.

**Linear Integration mode**

In the linear integration mode, the pixel is reset by turning on the reset transistor. After switching off the reset transistor, the rate of decay of the bias voltage on the diode is ideally [2],

$$\frac{dV}{dt} = \frac{1.2\lambda P \eta}{c}$$  \(\text{(1)}\)

where the factor 1.2 incorporates various constants and a proportional factor, $\lambda$ is the wavelength in microns, $P$ is the incident power in watts, $\eta$ is the quantum efficiency and $c$ is the velocity of light. After a certain integration time, the charge on the photodiode is readout through a in-pixel source follower amplifier by switching on the row select transistor. The output voltage is proportional to the light intensity and the integration time. It can be seen that the diode area is not present in Eq. (1) and the ideal response is independent of the diode area. However, in practice parasitic capacitance from the diode periphery and the FETs leads to an area dependence.

**Logarithmic mode**

By connecting the gate of reset transistor to $V_{DD}$ as shown in Fig. 2(b), the reset transistor operates in the weak inversion region. Thus, the current is dominated by diffusion of minority electrons from source to drain. The detected photocurrent ($I_{ph}$) is continuously converted to an output voltage, which can be shown to vary as,
\[ V_A = V_{DD} - \frac{kT}{q} \ln \left( \frac{I_{ph}}{I_0} \right) \] (2)

where \( V_A \) is the output voltage and \( I_0 \) is a constant. Owing the logarithmic response, this configuration has a large dynamic range. The absence of an integration time allows truly random access to the array. The drawback of this mode is its slow response at low light intensity and small output voltage swing, leading to a low signal-to-noise ratio [3].

**EXPERIMENTAL RESULTS**

The photo response of a test diode on the same chip is obtained by measuring the photocurrent at different wavelengths with applied reverse bias of 4 V. The normalized photo-response of the photodiode is shown in Fig. 6, from which can be seen that the relatively high response at green and yellow wavelengths decreases rapidly as the wavelength increases towards 1000 nm.

![Normalized photo-response of a 30 x 30 µm diode at reverse bias of 4 V.](image)

**Fig. 6** Normalized photo-response of a 30 x 30 µm diode at reverse bias of 4 V.

Fig. 7 shows how the output voltage (after correlated double sampling) changes with the light intensity at wavelengths of 660 nm and 850 nm. The array scan speed is about 400 kHz (i.e. pixel integration time of 2.5 ms). It shows a linear relation of output signal with light intensity.

![Output voltage of a typical pixel in the array after CDS at different light intensities with a pixel integration time of 2.5 ms at the indicated wavelengths.](image)

**Fig. 7** Output voltage of a typical pixel in the array after CDS at different light intensities with a pixel integration time of 2.5 ms at the indicated wavelengths.

The variation of output voltage with the integration time was measured by changing the frequency of the column readout clock, which affects the time interval between each pixel reset. The result is shown in Fig. 8. It exhibits a linear relationship at short integration times (< 3 ms), before the signal begins to saturate. Further increase of integration time causes the output voltage to fall. We believe this is due to the leakage current in the sample and hold capacitors when the storage time is large; further investigation is underway.

![Output voltage of a typical pixel in the array after CDS at different pixel integration times; wavelength of 660 nm with light intensity of 1.74 mW/cm².](image)

**Fig. 8** Output voltage of a typical pixel in the array after CDS at different pixel integration times; wavelength of 660 nm with light intensity of 1.74 mW/cm².

In this design, the same array can be operated in a logarithmic mode to achieve a wide dynamic range [3]. Fig. 9 shows the experimental results covering 3 orders of magnitude of light intensity. The result is comparable to that of commercial product. However, compared with the linear integration mode, logarithmic operation has a low output voltage swing and thus low signal-to-noise ratio [4].
CONCLUSIONS

A 4 x 64 array of CMOS active photodiodes with on-chip timing and control has been fabricated using a 0.5 µm process (shown in Fig. 10). The sensor can be operated in either a linear integration mode or logarithmic mode. The experimental results show that this image sensor has good linearity. It also achieves wide dynamic range in the logarithmic mode operation.

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REFERENCES


