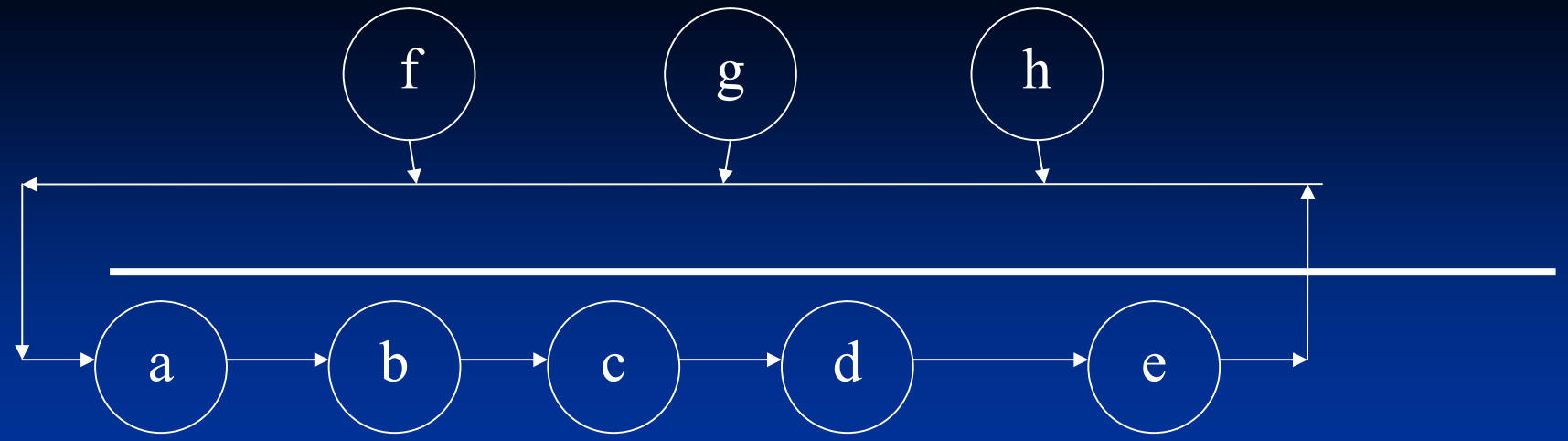
Advanced Digital Logic Design

ASM

Counters and Controllers

- Counters move from a state to another state.
- Controllers can be represented by counters
- Example: Vending machine controller, or traffic light controller



D_C

1	1	1	1
	1		1

D_B

	1		
1	1		

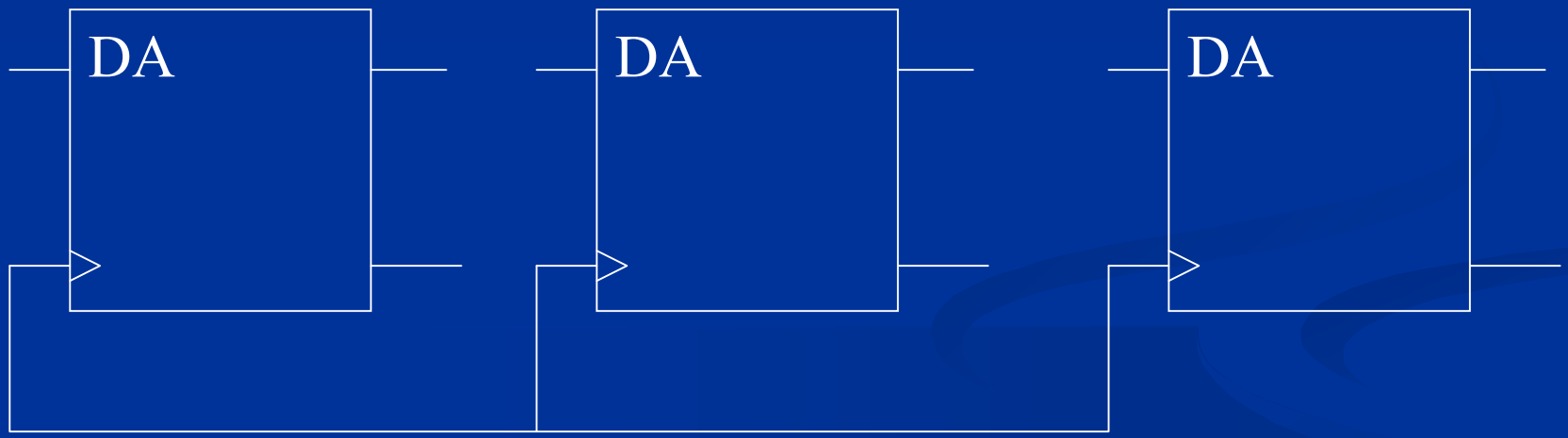
Current	next	A	B	C
000	001	0	0	1
001	010	0	1	0
010	011	1	1	1
011	111	1	1	1
100	001	0	0	1
101	001	0	0	1
110	001	0	0	1
111	100	1	0	0

D_A

	B		
	1	1	

C

A


DA
DA
DA

Glitch

- Glitch is an undesirable logic level that occurs during a short period of time.
- Example 111→ 110

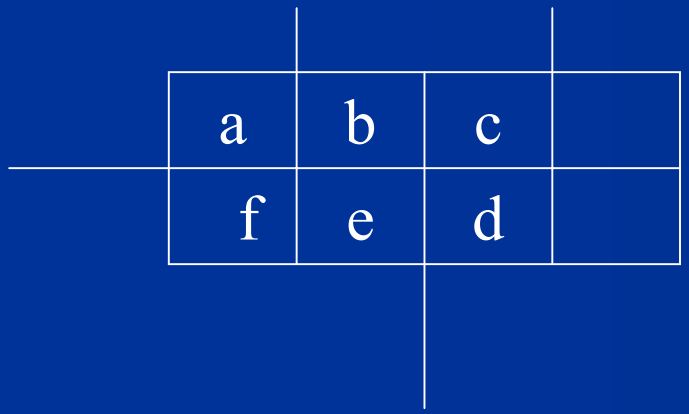
Glitches

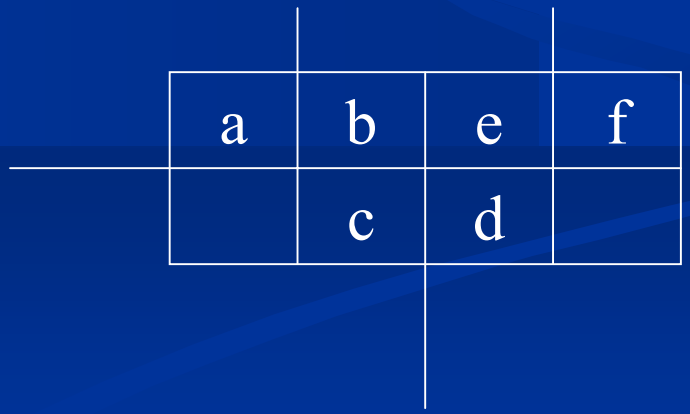
- Glitch free design
- Hazard protection: Circuit is designed such that glitches does not create errors
- Glitch tolerant circuits: If glitches do not affect the circuit, for example in driving a stepper motor, it takes milliseconds to move, glitches in the order of nanoseconds do not affect the motor

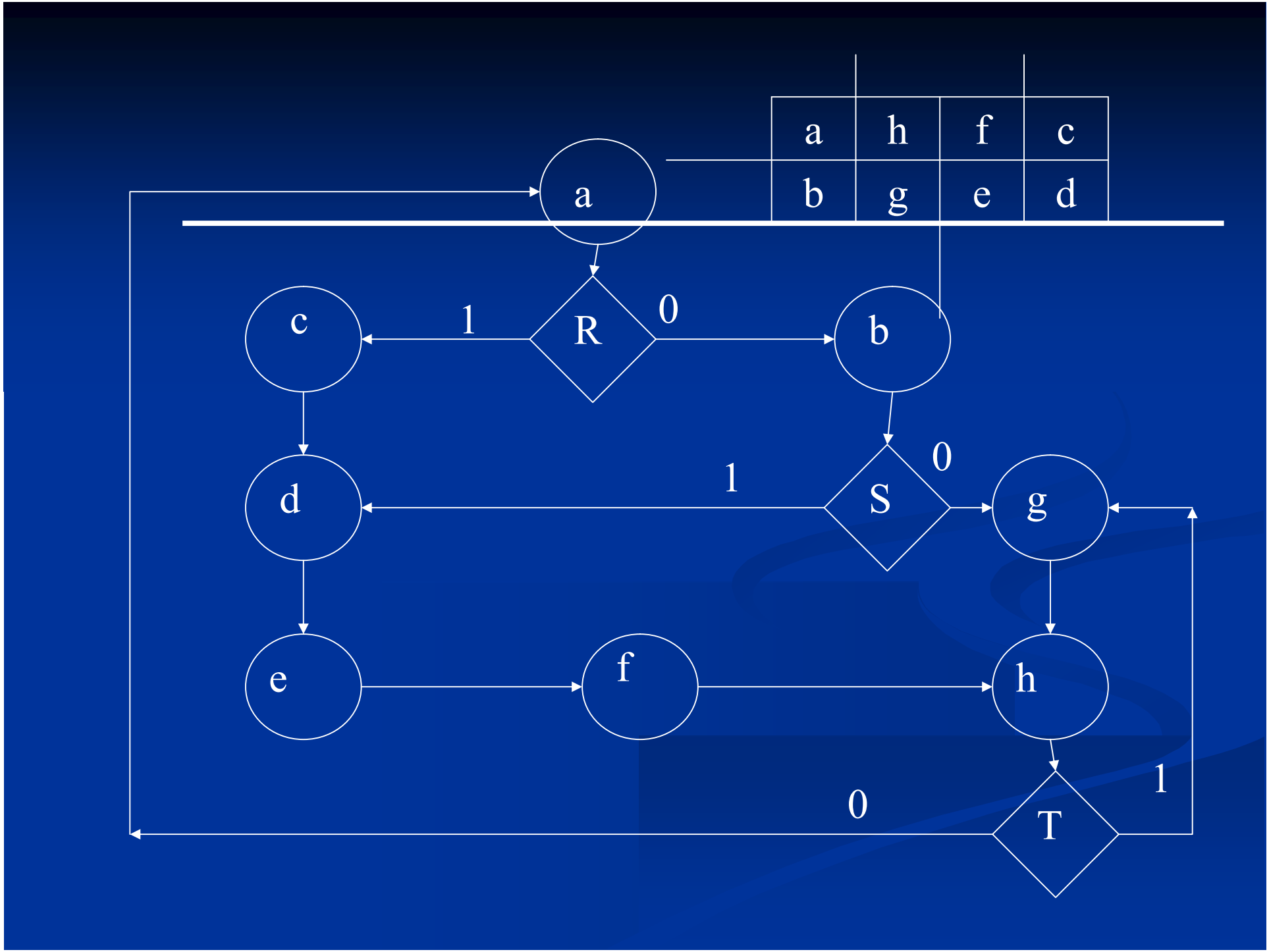
Glitches

- Glitch free design: Gray codes

a b c d e f



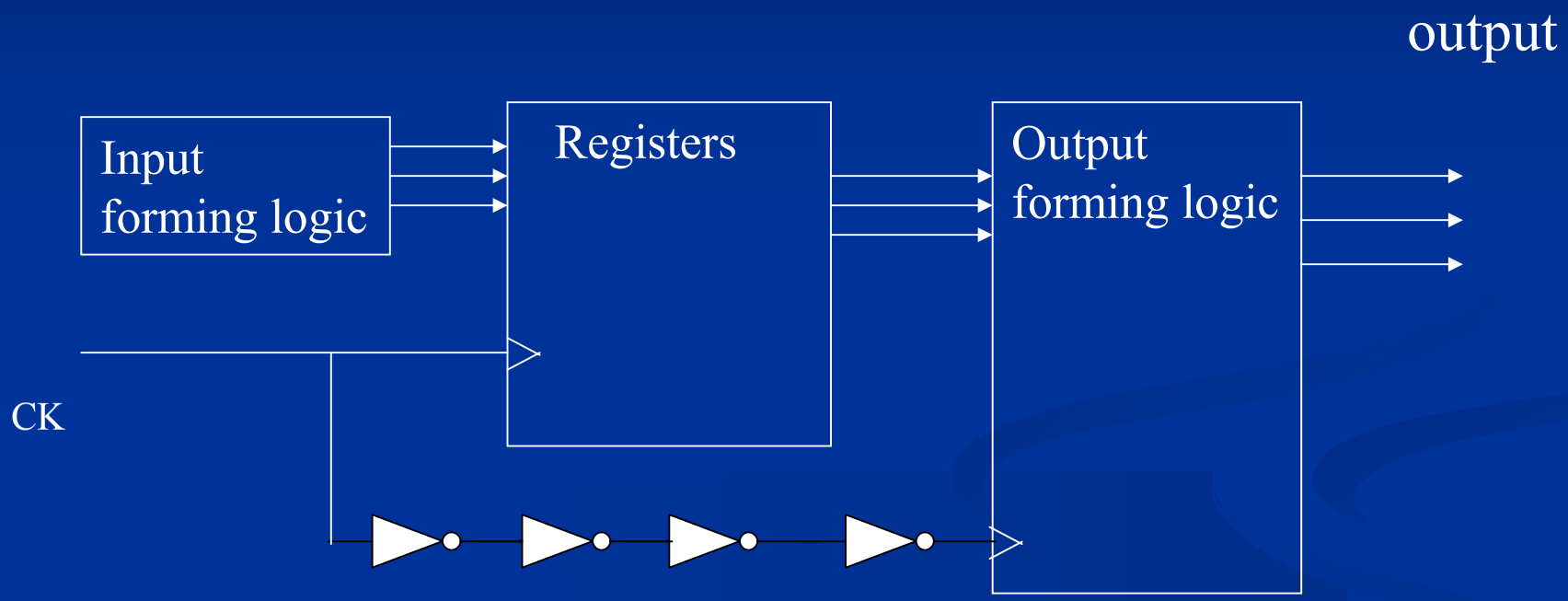



a h f c
b g e d
a
R
1
0
c
b
d
S
1
0
g
e
f
h
T
0
1

Glitches

- Some times it is not possible to use Gray codes, for example any odd number of states in a cycle.
- We can use delayed state timing, or Alternate state timing

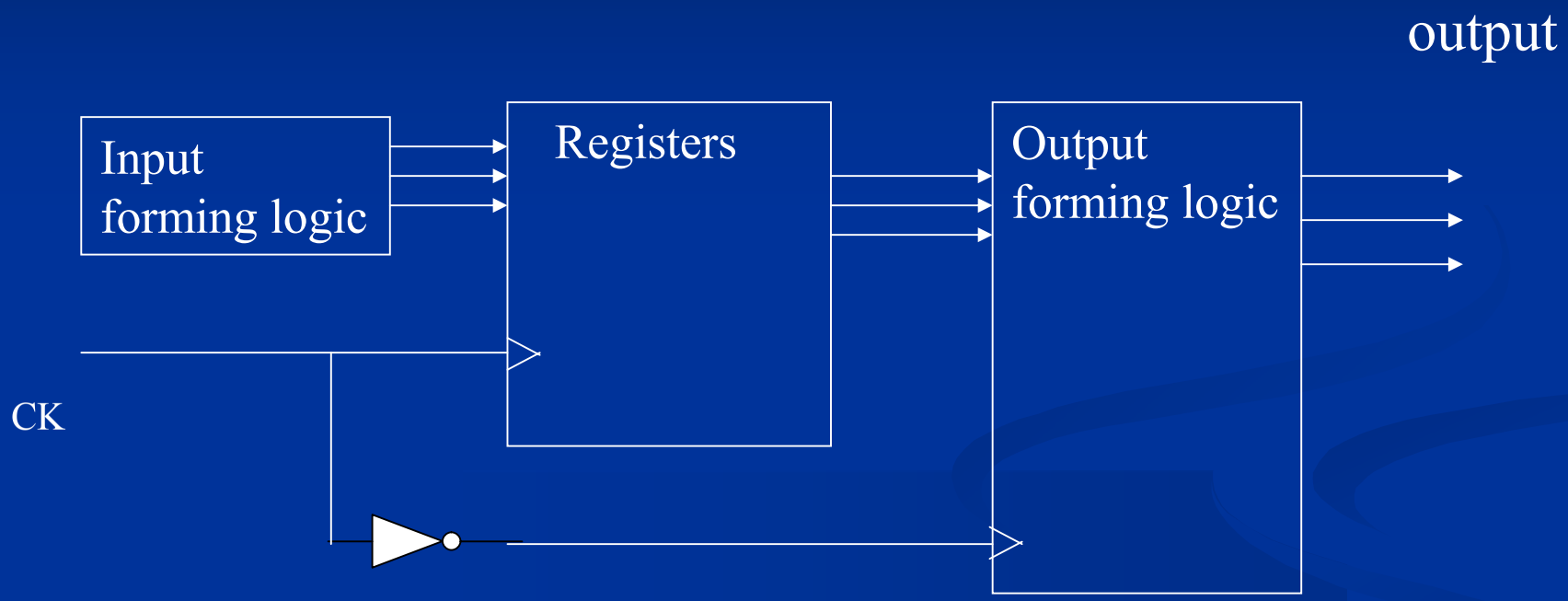
Delayed state timing



Assumption: output forming logic is enabled by CK

Must analyze the circuit to calculate how much delay we need

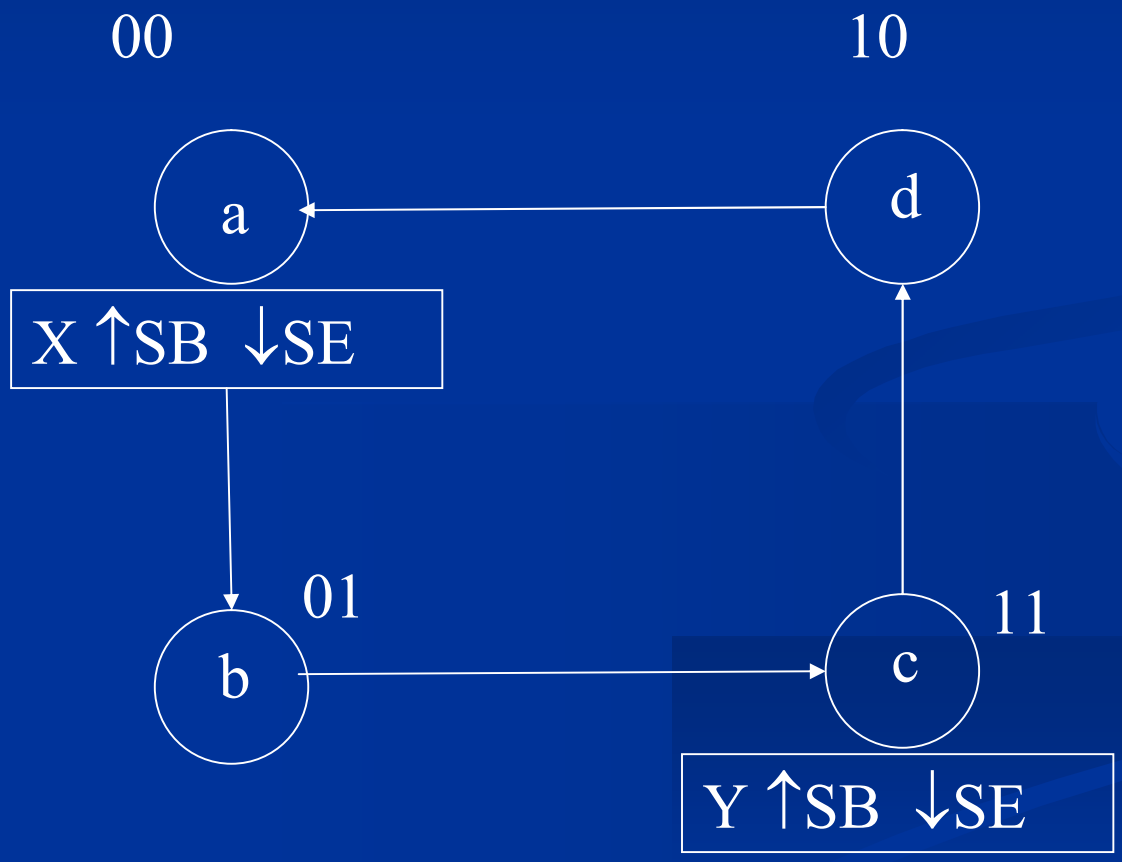
Alternate State Timing

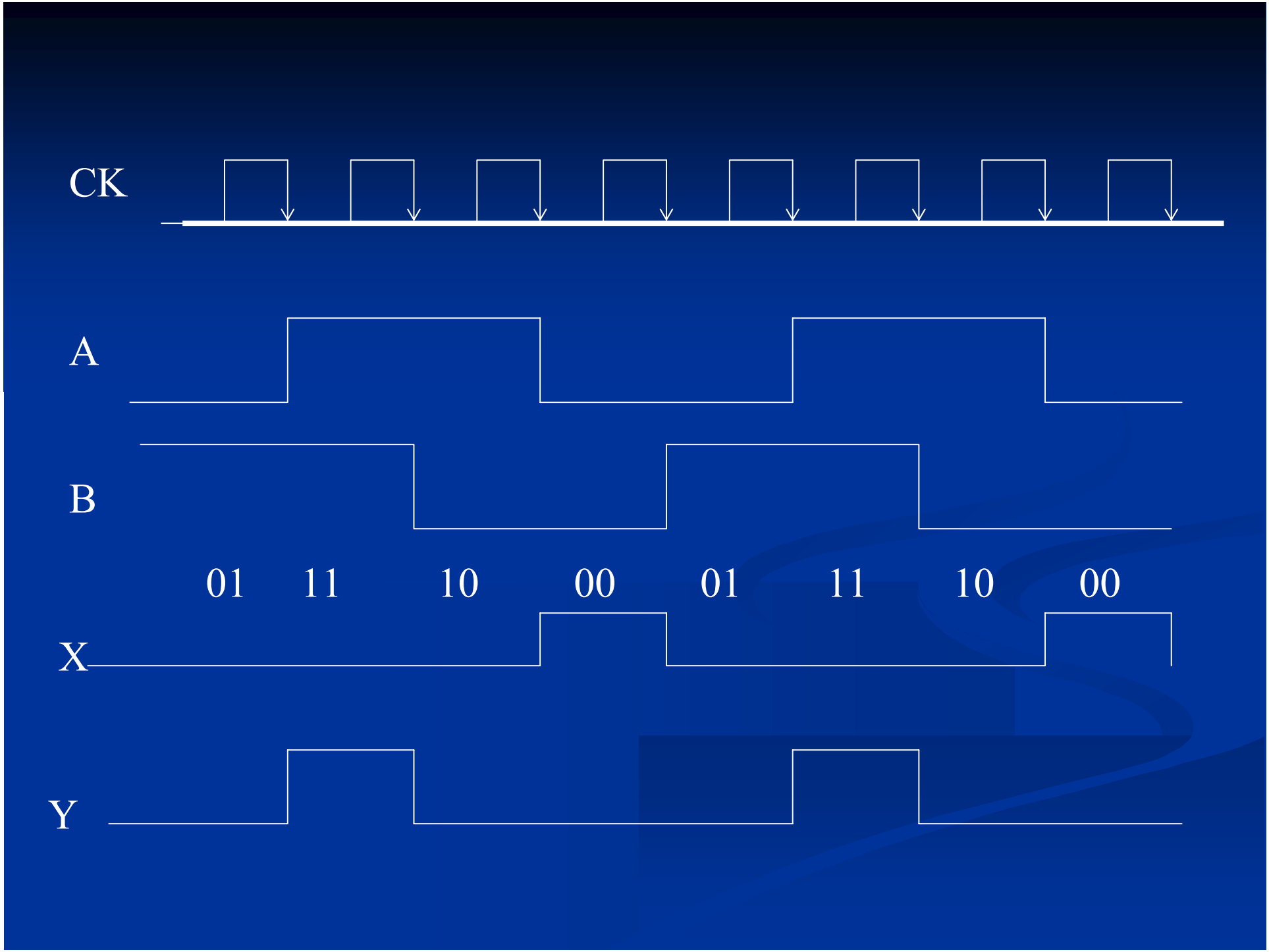


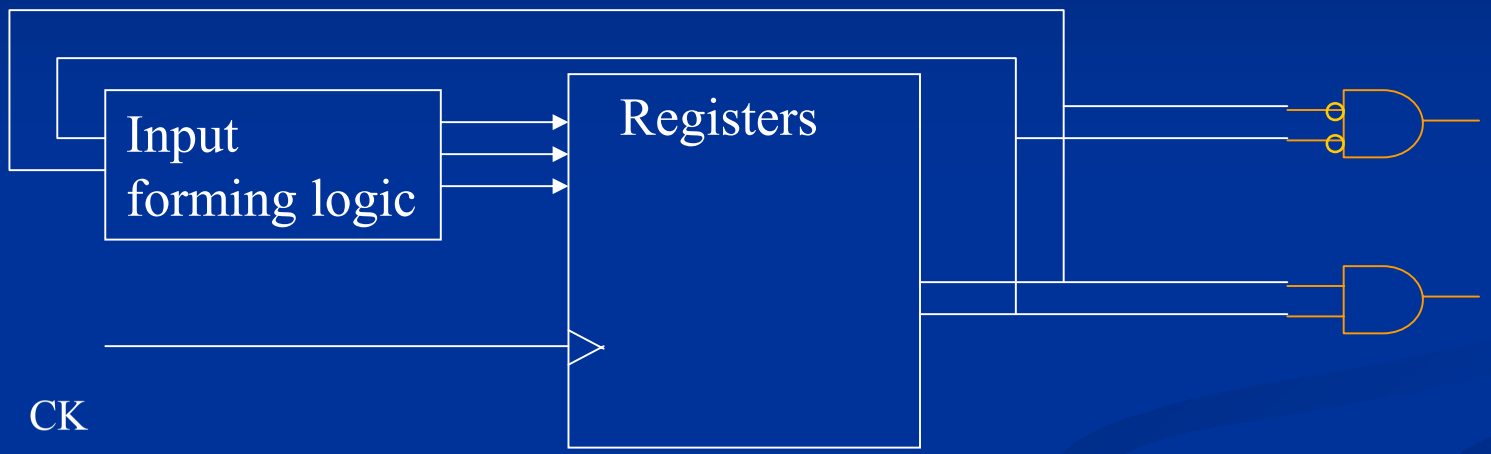
Delay the clock by half a cycle

Output logic is enabled at the rising edge (registers at the falling edge ----- Synchronous and predictable

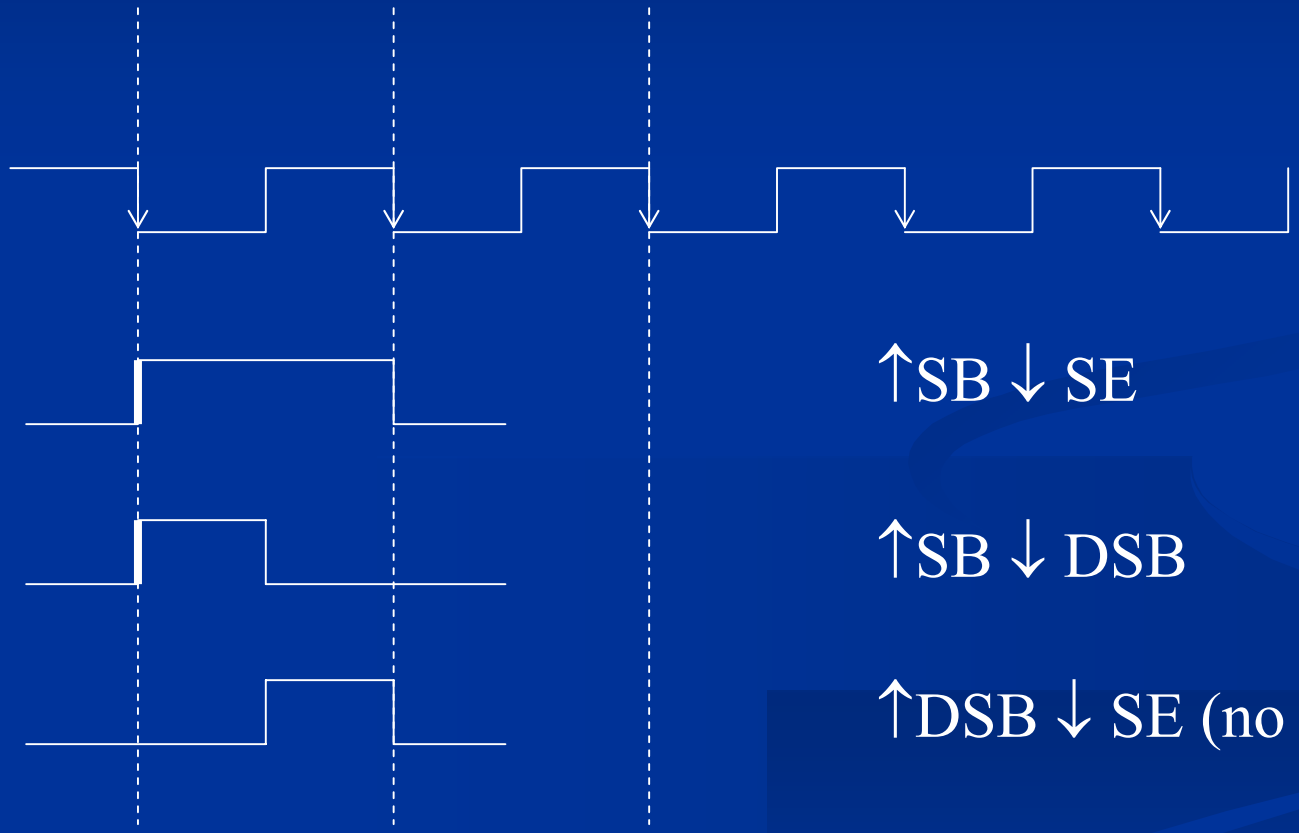
Output Forming Logic




CK
A
B
01
11
10
00
01
11
10
00
X
Y


Input
forming logic
Registers
CK

Output Forming Logic



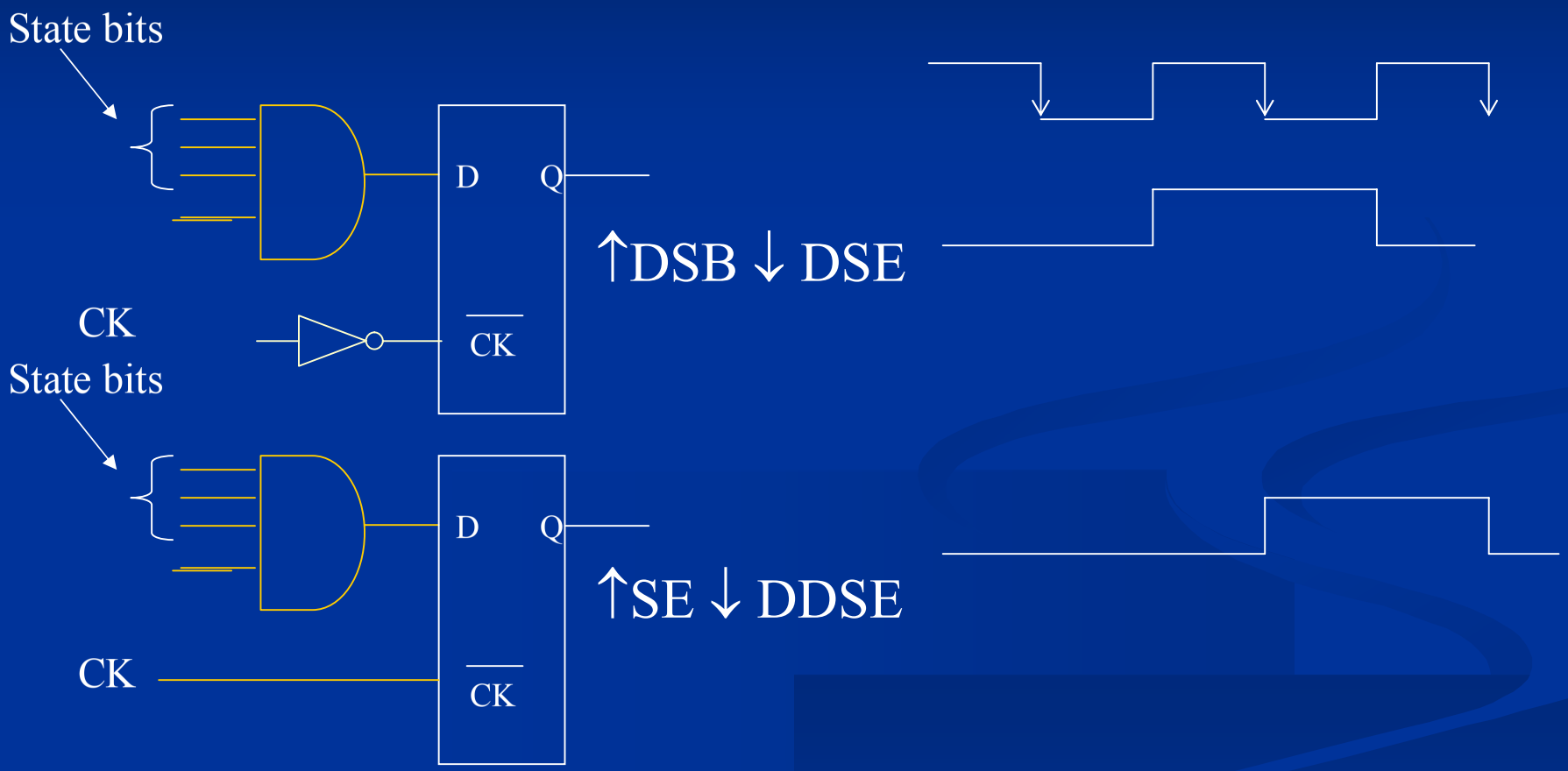
↑SB ↓ SE

↑SB ↓ DSB

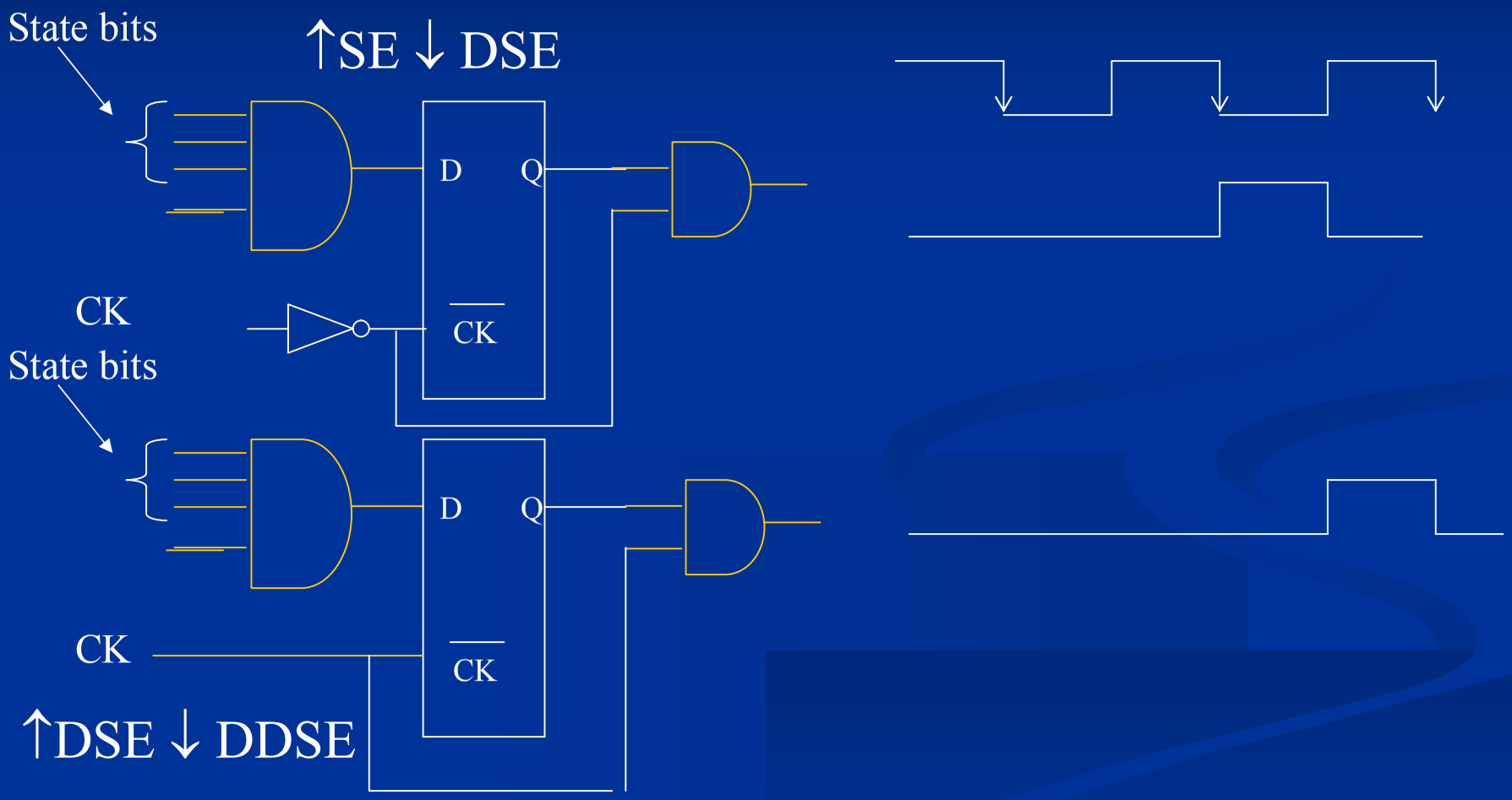
↑DSB ↓ SE (no glitch)

Output Forming Logic

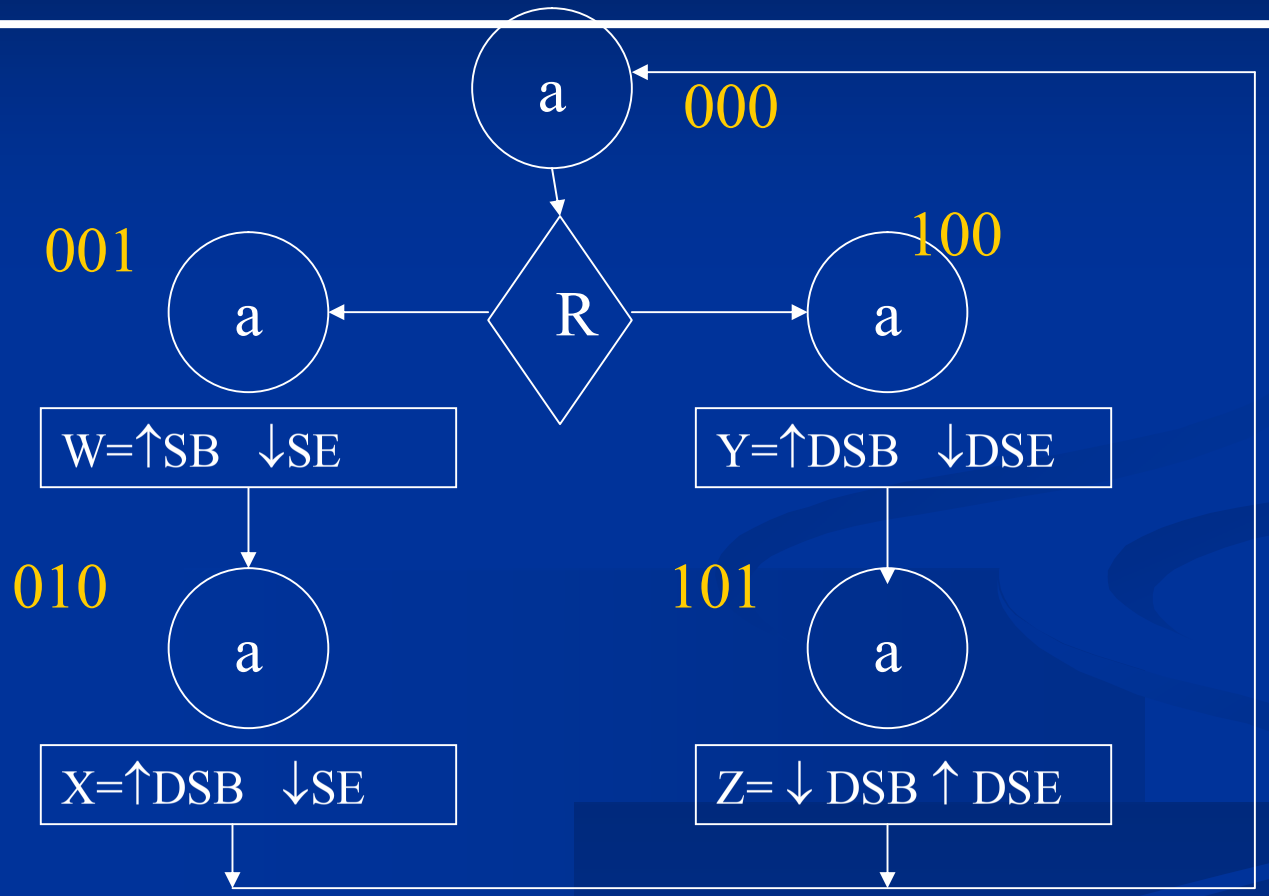
Output Forming Logic



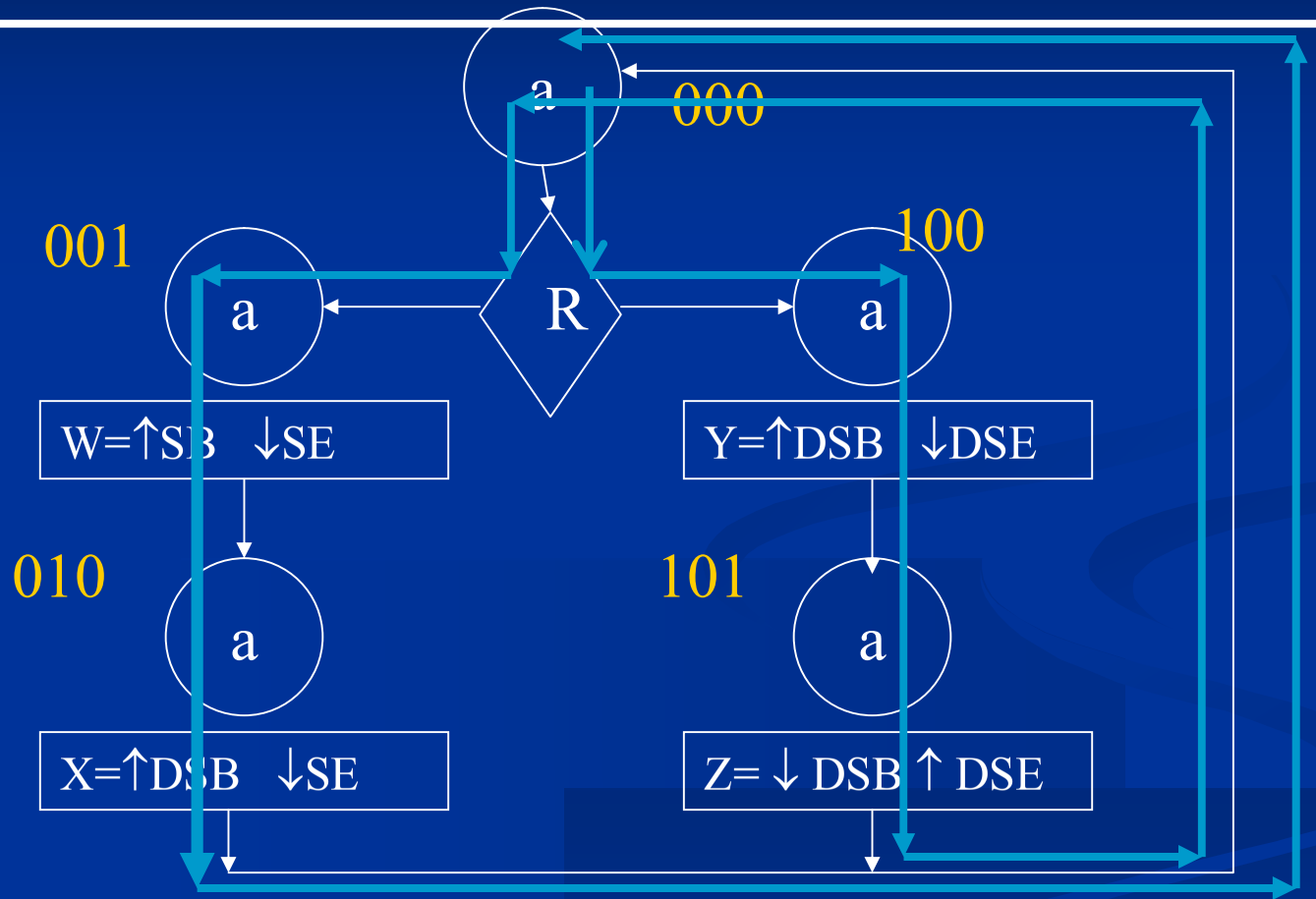
Output Forming Logic



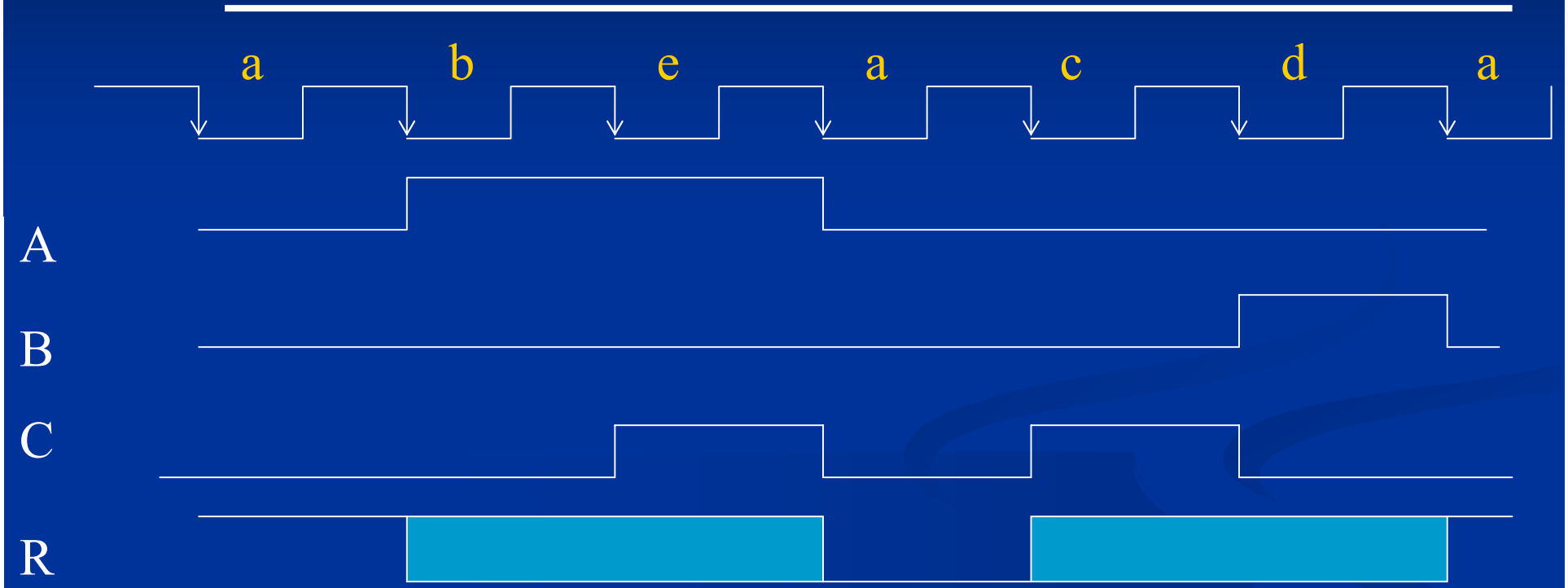
Example



Parsing



Timing Diagram



Example

	ABC	W	X	Y
B	000			
D	001			Y ↑SE
A	010	W ↑DSB		
C	011	W ↓SE	X ↑DSB	
F	110			Y↓DSB
E	111		X ↓DSE	

Conditional Output Forming Logic